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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,452	12/30/1999	ANAND MURTHY	042390.P7794	6341

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EXAMINER

LEE, EUGENE

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



Office Action Summary	Application No. 09/475,452	Applicant(s) MURTHY ET AL.	
	Examiner Eugene Lee	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 1 and 13 are objected to because of the following informalities: in line 1 of said claims, the word "An" should be changed to "a". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 8, 9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Gualandris et al. 5,041,885. Gualandris discloses (see, for example, FIG. 4) a field effect transistor (device) comprising a gate oxide (gate dielectric) 2, silicon substrate having an electrical conductivity of a first type (first conductivity region of a substrate) 5, gate electrode 1, oxide spacers (pair of sidewall spacers) 6, and source and drain regions of a polarity opposite to the polarity of the silicon substrate (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate) 7. The source and drain regions 7 are inwardly concaved and bend (inflection points) directly underneath the gate electrode 1. The channel region 5 directly beneath the gate electrode is larger than the channel region between the inflection points.

Regarding claims 8 and 9, see column 4, lines 64-66, wherein Gualandris discloses doping with a p-type conductivity like boron or with an n-type conductivity like arsenic-phosphorus.

Regarding claim 12, see FIG. 4 wherein Gualandris discloses a silicide 8 on source and drain regions 7.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. 5,041,885 as applied to claims 1, 8, 9 and 12 above, and further in view of Takeuchi 5,970,351. Gualandris does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi discloses (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B with a facet structure. In column 12, lines 45-63, Takeuchi teaches that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use this structure in Gualandris's invention in order to reduce parasitic capacitance.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. '885 as applied to claims 1, 8, 9 and 12 above, and further in view of Choi 6,057,582.

Gualandris does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in Gualandris's invention in order to reduce hot carrier effects.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. '885 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi 6,057,582. Gualandris in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in order to reduce hot carrier effects.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. 5,041,885 as applied to claims 1, 8, 9 and 12 above, and further in view of Choi

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et al. 5,793,088. Gualandris does not disclose a pair of deposited silicon or silicon alloy regions having a first conductivity type formed between said pair of deposited silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region. However, Choi discloses (see, for example, FIG. 2 and FIG. 3) a structure 106 comprising halo regions 120, 122. Choi teaches that halo regions provide higher punchthrough voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use halo regions in order to attain a higher punchthrough voltage.

9. Claims 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. 5,041,885. Gualandris does not disclose an inflection point which occurs between 50-200 Å laterally beneath said gate electrode and at a depth of between 25-200 Å beneath said gate dielectric. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these depths in order to form an adequate channel underneath the gate electrode, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 10 and 11, Krivokapic does not disclose the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type having a concentration between $1 \times 10^{18} / \text{cm}^3$ – $3 \times 10^{21} / \text{cm}^3$ or approximately $1 \times 10^{21} / \text{cm}^3$. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these concentrations in order to form source and drain regions that are capable of forming a channel therebetween, and since it has been held that where the general conditions

of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. 5,041,885 in view of Wieczorek et al. 6,274,894 B1 and further in view of Takeuchi 5,970,351. Gualandris discloses (see, for example, FIG. 4) a field effect transistor (device) comprising a gate oxide (gate dielectric) 2, silicon substrate having an electrical semiconductivity of a first type (first conductivity type region of a substrate) 5, gate electrode 1, oxide spacers (pair of sidewall spacers) 6, and source and drain regions of a polarity opposite to the polarity of the silicon substrate (a pair of source/drain regions having a second conductivity type formed in said substrate) 7. The source and drain regions 7 are inwardly concaved and bend (inflection points) directly underneath the gate electrode 1. Gualandris does not disclose silicon-germanium alloy source/drain regions. However, Wieczorek discloses (see, for example, column 6, lines 8-23) that SiGe (silicon-germanium) in the source/drain regions have a lower bandgap, which lowers contact resistance. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use silicon-germanium alloy in the source/drain regions of Gualandris in order to lower contact resistance.

Gualandris in view of Wieczorek does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi discloses (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B with a facet structure. In column 12, lines 45-63, Takeuchi teaches

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that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use this structure in Gualandris in view of Wieczorek in order to reduce parasitic capacitance.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gualandris et al. '885 in view of Wieczorek et al. '894 B1 in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi 6,057,582. Gualandris in view of Wieczorek in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film in order to reduce hot carrier effects.

Response to Arguments

12. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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Eugene Lee
January 15, 2004

Tom Thoms